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09/829,169	04/09/2001	Stephen C. Vincent	P04860US0	8267

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MCKEE, VOORHEES & SEASE, P.L.C.
801 GRAND AVENUE
SUITE 3200
DES MOINES, IA 50309-2721

EXAMINER

MCDONALD, RODNEY GLENN

ART UNIT PAPER NUMBER

1753

DATE MAILED: 02/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/829,169

Applicant(s)

VINCENT, STEPHEN C.

Examiner

Rodney G. McDonald

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 November 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5, 15 and 16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5, 15 and 16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Copetti et al. (US 2001/0017770) in view of Young et al. (U.S. Pat. 4,002,542) and DerMarderosian, Jr. (U.S. Pat. 5,076,906) or Nakamura et al. (U.S. Pat. 5,940,110).

Copetti et al. teach a module provided with a thin-film circuit. To realize the module with thin-film circuit, capacitors, or capacitors and **resistors (i.e. plural resistors)**, or capacitors, **resistors** and inductors are provided next to the conductor tracks directly on a substrate (1) of an insulating material. The partial or full integration of passive elements leads to the creation of a module which requires little space. (See Abstract)

Copetti et al. teach that their invention relates to a module for electronic device usable in TV sets and video recorder. (This indicates utilizing the layered material as chip usage) (Page 1 paragraph [0001, 0002, 0003])

In Fig. 1 the module with a thin-film circuit has **a substrate 1** which comprises a ceramic material, a glass-ceramic material, a glass material or a ceramic material. **A barrier layer 8 may be provided on the substrate 1. A resistance layer 7 is deposited on the substrate 1 or the barrier layer 8. This structured resistance**

layer 7 may comprise $Ni_xCr_yAl_z$ ($0 < x < 1$; $0 < y < 1$; $0 < z < 1$). A first electrically conductive layer 2 is provided on this resistance layer 7 and is structured. **A dielectric 3 is present on this structured first electrically conducting layer L, which dielectric 3 will normally cover the entire surface area of the substrate 1** and is interrupted in certain locations only so as to create vias to the subadjacent first structure electrically conducting layer 2. **The dielectric 3 may comprise Ta_2O_5 .** The first electrically conducting layer 2 may comprise Cu, Al, Al doped with a few percents of Cu, Al doped with a few percents of Si, Al doped with a few percents of Mg, or Al doped with a few percents of Cu and Si. (Page 2 paragraph [0060]; Page 3 paragraph [0060])

The differences between the Copetti et al. and the present claims is that depositing the tantalum pentoxide without utilizing oxidation to deposit the film is not discussed, exposing the thin film chip resistors to powered moisture conditions is not discussed and observing failures due to electrolytic corrosion under powered moisture conditions is not discussed.

Young teach in Fig. 1 a dielectric substrate 10 to which is applied a non-tantalum electrically conductive film electrode 12. The material of the dielectric substrate 10 may be any suitable dielectric material such as glass, ceramic, glass-ceramics or the like. The material of the electrode 12 may be any electrically conductive material which is compatible with tantalum oxide as well as compatible with the method of applying a film of tantalum oxide thereto, such as for example as aluminum, chromium nichrome, or the like. (Column 2 lines 20-30)

The dielectric substrate-electrode composite of FIG. 1 is disposed on substrate holder 16 while a target of tantalum oxide 22 is disposed on target holder 20 within housing 18. Housing 18 is then sealed and a predetermined desired vacuum is drawn therein. The amount of vacuum drawn depends on the materials involved in the sputtering as well as, to some extent, on the electrical parameters of the various parts of the apparatus. A quantity of inert ionizable gas is then introduced into housing 18 reducing the vacuum to a predetermined desired level. One familiar with the art can readily select a suitable level of vacuum for a specific set of parameters. The ionizable gas may be any suitable inert ionizable gas such as argon, xenon, nitrogen, or the like. A plasma is then initiated by means of filament cathode 24, anode 26, and dc power sources 36 and 37, while suitable r-f energy is applied to target material 22 by r-f power source 38. If desired, magnetic coils 40 and 42 may be energized to focus the plasma. Under these described conditions, **target material 22 will be caused to sputter** and be applied over electrode 12 on substrate 10. When desired, a mask may be interposed over electrode 12 to pattern the application of the target material on electrode 12. Such a mask is not shown, however, its nature will be readily understood by one familiar with the art. **After a suitable sputtering period of time, a layer or film 44 of target material 22 will be applied to electrode 12 as illustrated in FIG. 3. As heretofore described, the target material for thin film capacitors will be tantalum oxide, Ta₂O₅, which will comprise the capacitor dielectric. Although the proceeding describes a process of r-f triode sputtering from a Ta₂O₅ target, layer or film 44 may be applied by reactive sputtering from a tantalum target, by electron beam**

evaporation from a Ta₂O₅ target, by r-f diode sputtering from a Ta₂O₅ target, or by like methods. (Column 2 lines 57-68; Column 3 lines 1-24)

The motivation for depositing the tantalum pentoxide layer through sputtering is that it allows for depositing a film without reduced electrical series resistance. (Column 1 lines 32-35)

DerMarderosian, Jr. teaches a procedure for detecting and documenting flaws in glassivation layers protecting the active device region of an integrated circuit. (See Abstract)

In a first embodiment the device is non-destructively tested by covering the encapsulation layer with an electrolytic solution including deionized water and sulfuric acid, and applying the more positive potential to the electrolytic solution. In a second embodiment, a device including nichrome metallization is destructively tested by covering the encapsulation layer with an electrolytic solution including deionized water and sulfuric acid, and applying the more negative potential to the electrolytic solution. In a third embodiment, a device including aluminum metallization is destructively tested by covering the encapsulation layer with an electrolytic solution including deionized water and sodium chloride, and applying the more negative potential to the electrolytic solution. (Column 2 lines 54-68)

The motivation for performing testing of resistors under powered moisture conditions is that it allows for providing for a test that is less costly, more accurate, less time consuming and does not involve the use of hazardous chemicals. (Column 3 lines 1-5)

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OR

Nakamura et al. teach testing resistive films in Fig. 13. Fig. 13 shows the results of electrolytic etching test in order to evaluate the resistance to corrosion. The test was performed as a "leaving-to-stand test" under the conditions that the temperature was 85 degrees C, the humidity was 85%, the head voltage was 5 V and the thermosensible paper was kept applied. It was confirmed that by tapering of the electrode, moisture, ions of the thermosensible paper, etc. were prevented from easy entry into the thermal head, whereby corrosion of the electrode and the like could be prevented with the result that the resistance to corrosion was improved. (Column 10 lines 63-68; Column 11 lines 1-14)

The motivation for utilizing a test to test the electrolytic corrosion resistance of resistive films is that it allows for determination if the passivation film is corrosion resistant. (Column 11 lines 1-14)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Copetti et al. by forming a layer without oxidation by sputtering a layer of tantalum pentaoxide as taught by Young et al., by exposing the thin film chip resistors to powered moisture conditions and observing failures due to electrolytic corrosion under powered moisture conditions as taught by DerMarderosian, Jr. or Nakamura et al. because it allows for depositing a film without reduced electrical series resistance, for providing for a test that is less costly, more accurate, less time consuming and does not involve the use of hazardous chemicals or for determination if the passivation film is corrosion resistant.

Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minami (U.S. Pat. 4,777,583) in view of Young et al. (U.S. Pat. 4,002,542) and DerMarderosian, Jr. (U.S. Pat. 5,076,906) or Nakamura et al. (U.S. Pat. 5,940,110).

Minami et al. in Figure 2 teach a representation of their invention. In Fig. 2 numerals 1, 2, 3, 4, 5, 6 represent a ceramic substrate, a glaze layer, a **heat-generating resistor**, a common electrode, an individual electrode and a protecting film, respectively. (Column 3 lines 55-60) A known alumina ceramic is used as the ceramic substrate. (Column 3 lines 60-61) The glaze layer 2 is partially formed on the ceramic substrate 1. (Column 4 lines 5-6) The **heat-generating resistors 3** and **electrodes 4 and 5** are formed to have shapes shown in Fig. 1. A number of independent rows of heat-generating resistors 3 are formed on the glaze layer 2 at small intervals t in the longitudinal direction, and electrodes 4 and 5 having a width W are formed on the glaze layer 2 at small intervals t in the longitudinal direction. (Column 4 lines 25-31)

Titanium, chromium silicate, tantalum silicate, and tantalum nitride may be used **as the heat-generating resistor 3** and it is generally preferred that the thickness of the heat-generating resistors 3 be 0.05 to 0.5 microns. Aluminum or gold is used as the material constituting the **electrodes 4 and 5**, and it is preferred that the thickness of the electrodes 4 and 5 be 0.5 to 2.0 microns. (Column 4 lines 63-68; Column 5 lines 1-2) A **protecting film 6** may be formed on the heat generating resistors 3 and the electrodes 4 and 5, as shown in Fig. 2. A material excellent in the oxygen barrier property, the thermal conductivity, the electrically insulating property and the abrasion resistance,

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such as ***tantalum pentoxide***, is used for protecting film 6, and the thickness of the protecting film 6 is ordinarily 1.0 to 8.0 microns. (Column 5 lines 45-52)

The differences between Minami et al. and the present claims is the depositing of the layers is not discussed, where electrodes 4a and 5a are terminations is not discussed, depositing without oxidation and exposing the thin film chip resistors to powered moisture conditions and observing failures due to electrolytic corrosion under powered moisture conditions is not discussed.

As to the depositing the layers are deposited in order to achieve the structure of Figure 2 and must be deposited in that order such that the layers overlay one another. (See Figure 2)

As to the terminations since 4a and 5a are electrodes they are the terminations of the structure which are on the ends of the metal film as seen in Figs. 1 and 2. (See Figures 1 and 2)

Young et al. is discussed above and teach depositing without oxidation by sputtering. (See Young et al. discussed above)

The motivation for depositing without oxidation through sputtering is that it allows for depositing a film without reduced electrical series resistance. (See Young et al. discussed above)

As to the reduction of failures due to electrolytic corrosion under powered moisture conditions, it is believed that since tantalum pentoxide serves as a protective film it will protect the layers from moisture and corrosion. (See Column 5 lines 45-52)

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DerMarderosian, Jr. is discussed above and all is as applies above. (See DerMarderosian, Jr. discussed above)

The motivation for performing testing of resistors under powered moisture conditions is that it allows for providing for a test that it less costly, more accurate, less time consuming and does not involve the use of hazardous chemicals. (See DerMarderosian, Jr. Column 3 lines 1-5)

OR

Nakamura et al. is discussed above and all is as applies above. (See Nakamura et al. discussed above)

The motivation for utilizing a test to test the electrolytic corrosion resistance of resistive films is that it allows for determination if the passivation film is corrosion resistant. (Nakamura et al. Column 11 lines 1-14)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed a thin film resistor with moisture barrier layer as taught by Minami et al. and to have modified Minami et al. by depositing without oxidation through sputtering as taught by Young et al. and to have by exposed the thin film chip resistors to powered moisture conditions and observing failures due to electrolytic corrosion under powered moisture conditions as taught by DerMarderosian, Jr. or Nakamura et al. because it allows for depositing a film without reduced electrical series resistance, utilizing resistors to form thermal heads, for providing for a test that it less costly, more accurate, less time consuming and does not involve the use of hazardous chemicals or for determination if the passivation film is corrosion resistant.

Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minami et al. in view of Young et al., DerMarderosian, Jr. or Nakamura et al. as applied to claims 1 and 2 above, and further in view of Oki Electric Ind Co Ltd (Japan 52-3196).

The difference not yet discussed is the resistance layer being NiCr.

Minami et al. recognize that resistance layers to be used can be Ti and tantalum nitride, etc. (See Minami et al.)

Oki Electric Co. Ltd. Also recognize that resistance layers can be tantalum nitride, NiCr, etc. (See Oki Electric Co. Ltd. Abstract)

The motivation for replacing Minami et al.'s resistive layer with NiCr of Oki is that it allows for providing a layer with the required resistance feature. (See Abstract)

Therefore, it would have been obvious to one of ordinary skill in the art to have modified Minami et al. by replacing their resistive layer with a layer of NiCr as taught by Oki Electric Co. Ltd. because the resistive layers are art recognized equivalents.

Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over in Fuyama et al. (U.S. Pat. 4,617,575) view of DerMarderosian, Jr. (U.S. Pat. 5,076,906) or Nakamura et al. (U.S. Pat. 5,940,110) and Sato (Japan 61-27264) and Oki Electric Ind Co Ltd (Japan 52-3196).

Fuyama et al. teach in Fig. 1 **a heating resistor 110** of chromium silicon alloy having a thickness of 0.1 microns and first layer conductor 120 consisting of a chromium layer 10 and an aluminum layer 20 are formed in a predetermined pattern on an alumina substrate 100 with a glaze layer as an insulating substrate. Then, a protective film 140 made of silicon dioxide and serving as an insulating film at the same

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time is formed thereon throughout the entire surface by **sputtering** or plasma CVD so far used, preferably, to a thickness of about 3 microns. Then, a silicon nitride film 150 is formed only on the heating resistor 110 by mask plasma CVD. Crack formation can be prevented by the release of the stress on the silicon nitride. (Column 4 lines 19-35)

Tantalum pentoxide can be used alternatively to the silicon nitride. (Column 3 lines 30-33)

The differences between Fuyama et al. and the present claims is that depositing the films without oxidation of Ta is not discussed, the resistive film being a metal film is not discussed and exposing the thin film chip resistors to powered moisture conditions and observing failures due to electrolytic corrosion under powered moisture conditions is not discussed.

DerMarderosian, Jr. is discussed above and all is as applies above. (See DerMarderosian, Jr. discussed above)

The motivation for performing testing of resistors under powered moisture conditions is that it allows for providing for a test that it less costly, more accurate, less time consuming and does not involve the use of hazardous chemicals. (See DerMarderosian, Jr. Column 3 lines 1-5)

OR

Nakamura et al. is discussed above and all is as applies above. (See Nakamura et al. discussed above)

The motivation for utilizing a test to test the electrolytic corrosion resistance of resistive films is that it allows for determination if the passivation film is corrosion resistant. (Nakamura et al. Column 11 lines 1-14)

Sato teach in preparing a thermal head, ***an abrasion resistant layer 6 being a protective layer comprising tantalum pentoxide*** is formed in a thickness of about 5 microns by a sputtering method and heat-treated in air or a nitrogen atmosphere. This heat treatment is performed at a temperature equal to or higher than a peak temperature generated by the pulse driving or a heat generating resistor 2 to make it possible to impart a good characteristic for reducing the change ratio in the resistance value of the heat generating resistor 3. The relation of the resistance change ratio of thus formed thermal head and a pulse number is reduced in variation and stabilized over a long period of time and, because a heat treatment process is performed ***after each layer was formed by a sputtering method***, there is no interruption in the process and manufacturing cost can be reduced. (See Abstract)

The motivation for depositing each layer by a sputtering method is that it allows for no interruption in the manufacturing cost. (See Abstract)

Oki Electric Co. Ltd. teach that ***resistance layers can be metals such as W, NiCr***, etc. (See Oki Electric Co. Ltd. Abstract)

The motivation for utilizing resistance layers of metal is that it allows for providing a layer with the required resistance feature. (See Abstract)

As to the reduction of failures due to electrolytic corrosion under powered moisture conditions, since the tantalum pentoxide can be used as a protective layer it would protect against electrolytic corrosion. (See Fuyama et al. Column 3 lines 30-33)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Fuyama et al. by exposing the thin film chip resistors to powered moisture conditions and observing failures due to electrolytic corrosion under powered moisture conditions as taught by DerMarderosian, Jr. or Nakamura et al., by depositing the layers by sputtering as taught by Sato and to have utilized metals as the resistance layers as taught by Oki Electric Co. Ltd. because it allows for providing for a test that it less costly, more accurate, less time consuming and does not involve the use of hazardous chemicals or for determination if the passivation film is corrosion resistant and it allows for no interruption in the manufacturing cost and for providing a layer with the required resistance feature.

Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Copetti et al. (U.S. Pat. Pub. 2001/0017770) in view of Fuyama et al. (U.S. Pat. 4,617,575) and DerMarderosian, Jr. (U.S. Pat. 5,076,906) or Nakamura et al. (U.S. Pat. 5,940,110).

Copetti et al. is discussed above and all is as applies above. (See Copetti et al. discussed above)

The differences between Copetti et al. and the present claims is that depositing the without oxidation of the Ta is not discussed, depositing a layer of passivation on the substrate is not discussed and exposing the thin film chip resistors to powered moisture

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conditions and observing failures due to electrolytic corrosion under powered moisture conditions is not discussed.

Fuyama et al. is discussed above and teach depositing through sputtering and utilizing a passivation layer of silicon dioxide under a film of tantalum pentaoxide. (See Fuyama et al. discussed above)

The motivation for utilizing a layer of passivation under the film of tantalum pentaoxide is that it allows for serving as a protective and insulating film. (Column 4 lines 19-35)

DerMarderosian, Jr. is discussed above and all is as applies above. (See DerMarderosian, Jr. discussed above)

The motivation for performing testing of resistors under powered moisture conditions is that it allows for providing for a test that it less costly, more accurate, less time consuming and does not involve the use of hazardous chemicals. (See DerMarderosian, Jr. Column 3 lines 1-5)

OR

Nakamura et al. is discussed above and all is as applies above. (See Nakamura et al. discussed above)

The motivation for utilizing a test to test the electrolytic corrosion resistance of resistive films is that it allows for determination if the passivation film is corrosion resistant. (Nakamura et al. Column 11 lines 1-14)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Copetti et al. by utilizing a passivation

film as taught by Fuyama et al. and to expose the thin film chip resistors to powered moisture conditions and observing failures due to electrolytic corrosion under powered moisture conditions as taught by DerMarderosian, Jr. or Nakamura et al. because it allows for serving as a protective and insulating film and allows for providing for a test that is less costly, more accurate, less time consuming and does not involve the use of hazardous chemicals or for determination if the passivation film is corrosion resistant.

Response to Arguments

Applicant's arguments filed November 26, 2003 have been fully considered but they are not persuasive.

RESPONSE TO ARGUMENTS:

In response to the argument that Copetti et al. fails to teach discrete component thin film chip resistors, it is argued that Copetti et al. teach a separate or distinct (representing "discrete") component present on a "chip" which is a resistor comprised of a resistive thin film 7 and terminations 2. This is suggested in Figure 2 of Copetti et al. (See Figure 2 Copetti et al.) Furthermore Copetti et al. recognize that discrete components are preferred on the side of the substrate opposed to the thin film circuit and Copetti et al. recognize that "components" are resistors, inductors, capacitors, etc. (See Copetti et al. discussed above)

In response to the argument Copetti et al. fails to teach an outer moisture barrier layer that would protect the underlying layers from electrolytic corrosion, it is argued that Copetti et al.'s tantalum pentoxide layer is outer to the resistor and would protect the underlying layers. (See Copetti et al. discussed above)

In response to the argument that Copetti et al. fails to teach exposing thin film chip resistors to powered moisture conditions, it is argued that DerMarderosian, Jr. or Nakamura et al. teach subjecting resistive films to powered moisture conditions in order to detect deterioration in the resistor. (See DerMarderosian, Jr. or Nakamura et al. discussed above)

In response to the argument that neither DerMarderosian, Jr. nor Nakamura et al. fail to teach forming discrete component thin film chip resistors, it is argued that as discussed above Copetti et al. teach forming discrete component thin film chip resistors. DerMarderosian, Jr. nor Nakamura et al. teach subjecting resistor films to powered moisture conditions. (See Copetti et al., DerMarderosian, Jr. and Nakamura et al. discussed above)

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In response to the argument that the Examiner has not explained why electrolytic corrosion under powered moisture conditions would be of a particular interest to Copetti

et al., it is argued that the secondary references suggest that such powered moisture conditions will help in determining if the dielectric layer is corrosion resistant.

In response to the argument that Young fail to relate to discrete component thin film chip resistors, it is argued that Copetti et al. teach discrete component thin film chip resistors and that Young suggest depositing tantalum oxide films without oxidation. (See Copetti et al. and Young discussed above)

In response to the argument that Minami is not teach a discrete component thin film chip resistor, it is argued that Minami teach plural resistors as shown in Figure 4 as discrete components. (See Minami Figure 4)

In response to the argument that Oki does not teach the structural configuration, it is argued that the primary reference was relied upon to teach the structure configuration.

In response to the argument that Fuyama et al. do not teach the discrete component thin film chip resistor, it is argued that Fuyama et al. teach a discrete resistor in Figure 3. (See Figure 3 in Fuyama)

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within

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TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rodney G. McDonald whose telephone number is 571-272-1340. The examiner can normally be reached on M- Th with Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam X. Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Rodney G. McDonald
Primary Examiner
Art Unit 1753

RM
February 9, 2004